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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,071	11/13/2003	Toru Tominaga	36856.1141	6352
54066	7590	12/01/2005	EXAMINER	
MURATA MANUFACTURING COMPANY, LTD. C/O KEATING & BENNETT, LLP 8180 GREENSBORO DRIVE SUITE 850 MCLEAN, VA 22102			WILLOUGHBY, TERRENCE RONIQUE	
		ART UNIT		PAPER NUMBER
		2836		
DATE MAILED: 12/01/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/706,071	TOMINAGA ET AL.	
	Examiner Terrence R. Willoughby	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_\_.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-14 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-14 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    - a) All    b) Some \* c) None of:
      1. Certified copies of the priority documents have been received.
      2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
      3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | Paper No(s)/Mail Date: _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>11/13/03</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amano et al. (US 5,386,335) and in view of Kazuyoshi (JP 01-102884).

Regarding claim 1, Amano et al. discloses a surge absorber comprising: an insulator block (Fig. 18, 76) including a first internal electrode film (Fig. 14, 71) a second internal electrode film (Fig.14, 73), a ground external electrode layer (Fig.18, 80) provided on at least one side surface of the insulator block (Fig. 18, 76) so as to be connected with an end of the first internal electrode film (column 8, lines 10-13); and signal external electrode layers (Fig. 18, 78-79) provided on both end surfaces of the insulator block so as to be connected with both ends of the second internal electrode film (column 8, lines 7-10). Amano et al. lacks a discharge hole located in proximity to the first (Fig. 14, 71) and second (Fig.14, 73) internal electrode films.

However, Kazuyoshi discloses a discharge hole (Fig. 3, 26) located in the proximity of two internal opposing electrodes (Fig. 3, 22 and 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a discharge hole located in the proximity of two internal electrodes taught by Kazuyoshi between the first and second internal electrode films of Amano et al. to control the discharge voltage of the surge absorber due to the pressure of the inert gas between the two electrodes.

Regarding claim 2, Amano et al. in view of Kazuyoshi discloses a surge absorber according to claim 1, further comprising a resistor film (Amano et al., Fig. 17, 77) on at least one end surface of the insulator block (Amano et al., Fig. 17, 76), the resistor film being connected between one of the ends of the second internal electrode film and one of the signal external electrodes layers (Amano et al., column 8, lines 5-10).

Regarding claim 3, Amano et al. discloses a surge absorber array comprising: a insulator block (Fig. 28) including a fist internal electrode film (Fig. 28, 71), a plurality of second internal electrode films (Fig. 28, 93); a ground external electrode layer (Fig.31, 80) provided on at least one end surface of the insulator block (Fig. 18, 81) so as to be connected with an end of the first internal electrode film (column 10, lines 57-59); and signal external electrode layers (Fig. 31, 78-79) provided on both side surfaces of the insulator block so as to be independently connected with both ends of each of the second internal electrode films (column 10, lines 54-57). Amano et al. lack at least one

discharge hole located in proximity to the first internal electrode film (Fig. 14, 71) and the plurality of second internal films (Fig. 14, 73).

However, Kazuyoshi discloses a discharge hole (Fig. 3, 26) located in the proximity of two internal opposing electrodes (Fig. 3, 22 and 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a discharge hole located in the proximity of two internal electrodes taught by Kazuyoshi between the first internal electrode film and the plurality of second internal electrode films of Amano et al. to control the discharge voltage of the surge absorber due to the pressure of the inert gas between the two electrodes.

Regarding claim 4, Amano et al. in view of Kazuyoshi discloses the surge absorber according to claim 3 above, further comprising a resistor film (Amano et al., Fig. 17, ¶7) on at least one end surface of the insulator block the resistor film being connected between one of the ends of the second internal electrode film and one of the signal external electrode layers.

Regarding claim 5, Amano et al. discloses a surge absorber comprising: a laminated compact (Fig. 18, 76) of a first insulator sheet (Fig. 14, 72) having a first internal electrode film (Fig. 14, 71), a second insulator sheet (Fig. 14, 74) having a second internal electrode film (Fig. 14, 73); a ground external electrode layer (Fig. 18, 80) provided on at least one side surface of the laminated compact (Fig. 18, 81) so as

to be connected with an end of the first internal electrode film (column 8, lines 10-13); signal external electrode layers (Fig. 18, 78-79) provided on both end surfaces of the laminated compact so as to be connected with both ends of the second internal electrode film. Amano et al. lacks a ~~second~~ <sup>third</sup> insulator sheet having a discharge hole located in proximity to the first internal electrode film and the second internal electrode film.

However, Kazuyoshi discloses a discharge hole (Fig. 3, 26) located on a third insulator sheet (Fig. 3, 24), which is in close proximity of two internal opposing electrodes (Fig. 3, 22 and 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a third insulator sheet formed with a discharge hole, which is located in the proximity of two internal electrodes taught by Kazuyoshi between the first internal electrode film and the plurality of second internal electrode films of Amano et al. to control the discharge voltage of the surge absorber due to the pressure of the inert gas between the two electrodes.

Regarding claim 6, Amano et al. in view of Kazuyoshi discloses a surge absorber according to claim 5 above, further comprising a resistor film (Amano et al., Fig. 18, 77) on at least one end surface of the laminated compact (Amano et al., Fig. 18), the resistance film being connected between one of the ends of the second internal electrode film and one of the signal external electrode layers (Amano et al., column 8, lines 5-10).

Regarding claim 7, Amano et al. discloses a surge absorb array comprising: a laminated compact of a first insulator sheet (Fig. 14, 72) including a first internal electrode film (Fig. 14, 71), a second insulator sheet (Fig. 14, 74) having a plurality of second internal electrode films (Fig. 14, 71); a ground external electrode layer (Fig. 18, 80) provided on at least one end surface of the laminated compact (Fig. 18, 76) so as to be connected with an end of the first internal electrode film (column 8, lines 10-13); and signal external electrode layers (Fig. 18, 78-79) provided on both side surfaces of the laminated compact so as to be independently connected with both ends of each of the second internal electrode films. Amano et al. lack a third insulator sheet between the first and second insulator sheets (Fig. 14, numeral 72 and 74) having at least one discharge hole.

However, Kazuyoshi discloses a discharge hole (Fig. 3, 26) located on a third insulator sheet, which is the proximity of two internal opposing electrodes (Fig. 3, 22 and 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a third insulator formed with a discharge hole, which is in the proximity of two internal electrodes taught by Kazuyoshi between the first internal electrode film and the plurality of second internal electrode films of Amano et al. to control the discharge voltage of the surge absorber due to the pressure of the inert gas between the two electrodes.

Regarding claim 8, Amano et al. in view of Kazuyoshi discloses a surge absorber according to claim 7 above, further comprising a resistor film (Amano et al., Fig. 18, 77) on at least one end surface of the laminated compact (Amano et al., Fig. 18), the resistor film being connected between one of the ends of the second internal electrode film and one of the signal external electrodes layers (Amano et al., column 8, lines 5-10).

Regarding claim 9, Amano et al. discloses a surge absorber comprising: a laminated compact (Fig. 18,76) of a first insulator sheet (Fig. 14, 72) having a first internal electrode film (Fig. 14, 71), a second insulator sheet (Fig. 14, 74) having a second internal electrode film (Fig. 14, 73); a ground external electrode layer (Fig.18, 80) provided on at least one side surface of the laminated compact (Fig. 18, 81) so as to be connected with an end of the first internal electrode film (column 8, lines 10-13); signal external electrode layers (Fig. 18, 78-79) provided on both end surfaces of the laminated compact so as to be connected with both ends of the second internal electrode film. Amano et al. lacks a second insulator sheet having a discharge hole located in proximity to the first (Fig. 14, 71) and second (Fig.14, 73) internal electrode films.

However, Kazuyoshi discloses a discharge hole (Fig. 3, 26) located in the proximity of two internal opposing electrodes (Fig. 3, 22 and 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a

second insulator sheet having a discharge hole, which is located in the proximity of two internal electrodes taught by Kazuyoshi between the first internal electrode films and the second internal electrode film of Amano et al. to control the discharge voltage of the surge absorber due to the pressure of the inert gas between the two electrodes.

Regarding claim 10, Amano et al. in view of Kazuyoshi discloses a surge absorber according to claim 9 above, further comprising a resistor film (Amano et al., Fig. 18, 77) on at least one end surface of the laminated compact (Amano et al., Fig. 18), the resistance film being connected between one of the ends of the second internal electrode film and one of the signal external layers (Amano et al., column 8, lines 5-10).

Regarding claim 11, Amano et al. discloses a surge absorber comprising: a laminated compact (Fig. 18,76) of a first insulator sheet (Fig. 14, 72) having a first internal electrode film (Fig. 14, 71), a second insulator sheet (Fig. 14, 74) having a second internal electrode film (Fig. 14, 73), and a resistor film (Fig. 18, 77) provided on a surface of the laminated compact; a ground external electrode layer (Fig.18, 80) provided on at least one side surface of the laminated compact as to be connected with an end of the first internal electrode film (column 8, lines 10-13); a first signal external electrode layer (Fig. 18, 78) provided on one end surface of the laminated compact (Fig. 18, 76) so as to be connected with an end of the second internal electrode film and one end of the resistor film (Fig. 18, 77) ; and a second signal external electrode layer (Fig. 18, 79) provided on the other end surface of the laminated compact so as to be

connected with the other end of the resistor film (Fig. 18,77).Amano et al. lacks a third insulator sheet between the first and the second insulator sheets having a discharge hole.

However, Kazuyoshi discloses a discharge hole (Fig. 3, 26) located on a third insulator sheet, which is the proximity of two internal opposing electrodes (Fig. 3, 22 and 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a third insulator formed with a discharge hole, which is in the proximity of two internal electrodes taught by Kazuyoshi between the first and the second insulator sheets of Amano et al. to control the discharge voltage of the surge absorber due to the pressure of the inert gas between the two electrodes.

Regarding claim 12, Amano et al. in view of Kazuyoshi discloses a surge absorber according to claim 11, wherein the resistor film (Amano et al., Fig. 19, 77a) is asymmetrical (Amano et al., column 8, lines 50-58) in plain view with respect to a line extending between both sides surfaces (Amano et al., Fig. 19, 78-79) of the laminated compact (Amano et al. Fig. 19, 81a).

Regarding claim 13, Amano et al. discloses a surge absorber comprising: a laminated compact (Fig. 18,76) a first insulator sheet (Fig. 20, 72) having a first internal electrode film (Fig. 20, 71), a second insulator sheet (Fig. 20, 74) having a second internal electrode film (Fig. 20, 73), a fourth insulator sheet (Fig. 20, 82) having a

resistor film (Fig. 20, 77); a ground external electrode layer (Fig.18, 80) provided on at least one side surface of the laminated compact (Fig. 18,76) as to be connected with an end of the first internal electrode film (column 8, lines 10-13); a first signal external electrode layer (Fig. 18, 78) provided on one end surface of the laminated compact (Fig. 18, 76) so as to be connected with an end of the second internal electrode film and one end of the resistor film (Fig. 18, 77) ; and a second signal external electrode layer (Fig. 18, 79) provided on the other end surface of the laminated compact so as to be connected with the other end of the resistor film (Fig. 18,77). Amano et al. lacks a third insulator sheet between the first and the second insulator sheets having a discharge hole.

However, Kazuyoshi discloses a discharge hole (Fig. 3, 26) located on a third insulator sheet, which is the proximity of two internal opposing electrodes (Fig. 3, 22 and 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a third insulator formed with a discharge hole, which is in the proximity of two internal electrodes taught by Kazuyoshi between the first and the second insulator sheets of Amano et al. to control the discharge voltage of the surge absorber due to the pressure of the inert gas between the two electrodes.

Regarding claim 14, Amano et al. in view of Kazuyoshi discloses a surge absorber according to claim 13, wherein the resistor film wherein the resistor film (Amano et al., Fig. 19, 77a) is asymmetrical (Amano et al., column 8, lines 50-58) in

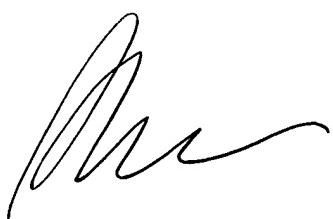
plain view with respect to a line extending between both sides surfaces (Amano et al., Fig. 19, 78-79) of the laminated compact (Amano et al. Fig. 19, 81a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terrence R. Willoughby whose telephone number is 571-272-2725. The examiner can normally be reached on 8-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PHUONG T. VU  
PRIMARY EXAMINER